SPONSORSHIP CERTIFICATE

Certified that Mr./Ms./Dr..... is an employee of our institute and is hereby sponsored for the FDP on "Selected Topics in VLSI Design and Embedded Systems", at C. V. Rama n College of Engineering, Bhubaneswar during the period 1st June to 13th June 2015.

He/She will be permitted to attend the course, if selected.

It is also certified that our institute is an AICTE approved institute.

Place: Name & Signature

Date:

(Director/Principal)

(Seal of the institution)

IMPORTANT INFORMATION

Selection will be on first come first serve basis subject to AICTE and CVRCE norms.

Last date for receipt of applications:
30-05-2015.

Intimation of selection:
on or before 30-05-2015.

ADDRESS FOR CORRESPONDENCE

Dr. P. Kabisatpathy, Coordinator
"FDP on STVDES'15", Department of ETC, CVRCE, Bidyanagar, Mahura, Janla, Bhubaneswar – 752054,
Phones: (O) 0674 – 2460093, 2460043
(M) 09437307944
Email : pkabisatpathy@gmail.com

ABOUT THE INSTITUTION (CVRCE)

C. V. Raman College of Engineering (CVRCE), extending over 100 acres of beautifull y landscaped area, situated o n the outskirts of Bhubaneswar, is a progressive Institution in Orissa, setup to promote the highest standards of technical education in the State. The Institute is approved by the All India Cou ncil for Technical Education. The Institute is also accredited by NBA and ce rtifies to ISO9001:20 08. The Institute is rated as "A" Grade Engineering College by NAAC and is affiliate d to Biju Patnaik University of Technology. The college aims at educating the students to become not only competent professionals but al so excellent human beings, who would contribute towards the welfare of the society and help in raising the quality of life of its people.

ABOUT THE DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

The Department is offering B. Tech in "Electronics & Telecommunication Engineering", M. Tech in "Electronics & Communication Engineering". The department is ca rrying out R&D and consultation activities in are as such as Adhoc Networks, Mobile Communication, Smart Antenna, Microwave Engine ering, Analog and Digital VLSI, Pattern Recognition, VLSI Implementation of DSP and Communication Systems, and Image Analysis an d Computer Vision. Apart from the re gular course curriculum, the department also imparts various industry oriented skill based training programs to educate and incorporate the fast-changing technological trends to its students an d other professionals in the field of Electroni cs and Telecommunication Engineering.

All India Council of Technical Education (AICTE), India

SPONSORED

FACULTY DEVELOPMENT PROGRAMME

ON

"Selected Topics in VLSI Design and Embedded Systems"

(01st June ~ 13th June 2015)

Coordinator

Dr. Prithviraj Kabisatpathy

Organized by

Department of Electronics & Telecommunication Engineering

C. V. Raman College of Engineering,

Bhubaneswar, Odisha, India

PREAMBLE

VLSI Design and Embedded Systems are an integral part of the curriculum under Biju Patnaik University of Technology, Rourkela, Odisha.

This FDP will expose the faculty members to recent advances in the field of Digital, Analogue and Mixed-Signal VLSI Design, Testing & Verification, Fault Diagnosis, VLSI Packaging, Floorplanning & Routing Methodologies, FPGA Design, Embedded System Design, SOC Design, MEMS and many more relevant subjects.

This FDP will help develop and establish faculty members in Research and Academic Activities.

COURSE CONTENT

Selected topics on VLSI and embedded system design.

Tentative contents:

- Semiconductor Device Characteristics
- Low Power and Low Voltage Techniques
- Embedded System Design
- ARM Processors
- ASIC Design
- Introduction to Xilinx ISE EDA
- Introduction to Mentor Graphics EDA
- Introduction to Cadence EDA
- Advances in Analog & RF Testing
- CORDIC Architectures

RESOURCE PERSONS

Sessions will be handled by faculty experts from IITs, NITs and reputed universities along with expert from industries.

WHO SHOULD ATTEND

Faculty from various AICTE approved Engineering colleges/ Institutions and working professionals from Industries/ Utilities/ R&D and other organizations with basic degree in Electrical/ Computer/ Information Technology/ Electronics & Communication / Instrumentation Engineering.

REGISTRATION FEE

a) No registration fee for Teachers from AICTE approved institutions / Colleges

b) Participants from Industries/ Utilities/ R&D / other organizations: Rs.3000/- (this includes registration, material, and working lunch only).

TA/DA

Road or sleeper class fare on the shortest route will be provided to the participants from AICTE approved institutions on production of actual tickets . Accommodation will be provided in CVRCE hostels on prior request.

HOW TO APPLY

Application in the attached format duly recommended/ sponsored by the authority concerned, should reach the coordinator (by post/ Email) on or before 30-05-2015. Participants are requested to inform the coordinator regarding accommodation and transport.

FOR FURTHER DETAILS CONTACT

Dr. P. Kabisatpathy 09437307944(M)
Coordinator pkabisatpathy@gmail.com
Prof. S. Nanda 08763005692(M)
Co-Coordinator nanda.swagat@gmail.com
Prof. J. Dash 09437747859(M)
Co-Coordinator jayashreedash123@gmail.com

REGISTRATION FORM

Selected Topics in
VLSI Design and Embedded Systems
01st June to 13th June 2015

Department of Electronics & Telecommunication Engineering,
C. V. Raman College of Engineering,
Bhubaneswar, Odisha, Pin.752054
(Use CAPITAL LETTERS only)

1. Name : _____
2. Date of Birth: _____ Gender: (M/F)
3. Designation:_____
4. Department : _____
5. Institution:_____
6. Academic qualification: _____
7. Area of specialization: _____
8. Experience in years:_____
9. Mobile no.: _____
10. Email id: _____
11. Address of correspondence:_____
_____
_____
Pin code: _____
12. Is Accommodation required: (Yes/No)
13. Is Transport required: (Yes/No)

The information furnished above is true to the best of my knowledge. I agree to abide by the rules and regulations governing the course. If selected, I shall attend the course for the entire duration.

Place:
Date: Signature of the Applicant