C.V. Raman Global University
ODISHA BHUBANESWAR INDIA

Course Name: Digital VLSI Design

Overview:

Digital VLSI Design course will enhance the knowledge of the students in the most important aspects of VLSI Technology. The course has been structured keeping in view the current development in the field of VLSI design and its effect on the society. The development of the course tries to address the gap between academic course curriculum and semiconductor industry expectations.

Participant Profile:

- Under graduate students of 3rd Semester B.Tech. and above of ECE, CSE, CS-IT, AIML, EE, EEE branches can undertake this course.

Contents:

- Introduction to Digital Electronics
- VLSI Design Flow: FPGA & ASICs
- Basic Concept of HDL code
- VHDL/Verilog Coding using Xilinx ISE
- VLSI Design Styles: FPGA, Gate Array, Standard Cell Based & Full Custom Designs.

Learning Target:

The Participants will be able to

- Identify the various steps in VLSI Design flow
- Understand and Differentiate between ASIC & FPGA Design flow.
- Understand and Difference in VLSI design styles: FPGA, Standards cell Design & Full Custom Design
- Understand the basic concepts and programming styles of VHDL/Verilog HDL and Application.
- Design a synthesizable RTL solution with all the design rules & optimization methodologies.
- Implement the synthesized design blocks on target Xilinx Device and optimize the design for the specifications.

Prerequisites:

- Digital Electronics circuits
- Basics of electronics

Evaluation:

- Theory & Practical Exam
- Quiz
- Project work based on Industrial Application.

Fee: 5500/-

Teaching & Learning Media:

- Multi-media presentation
- Live project demonstration

Time Duration:

- 36 Hours
- 6 Hours/Day